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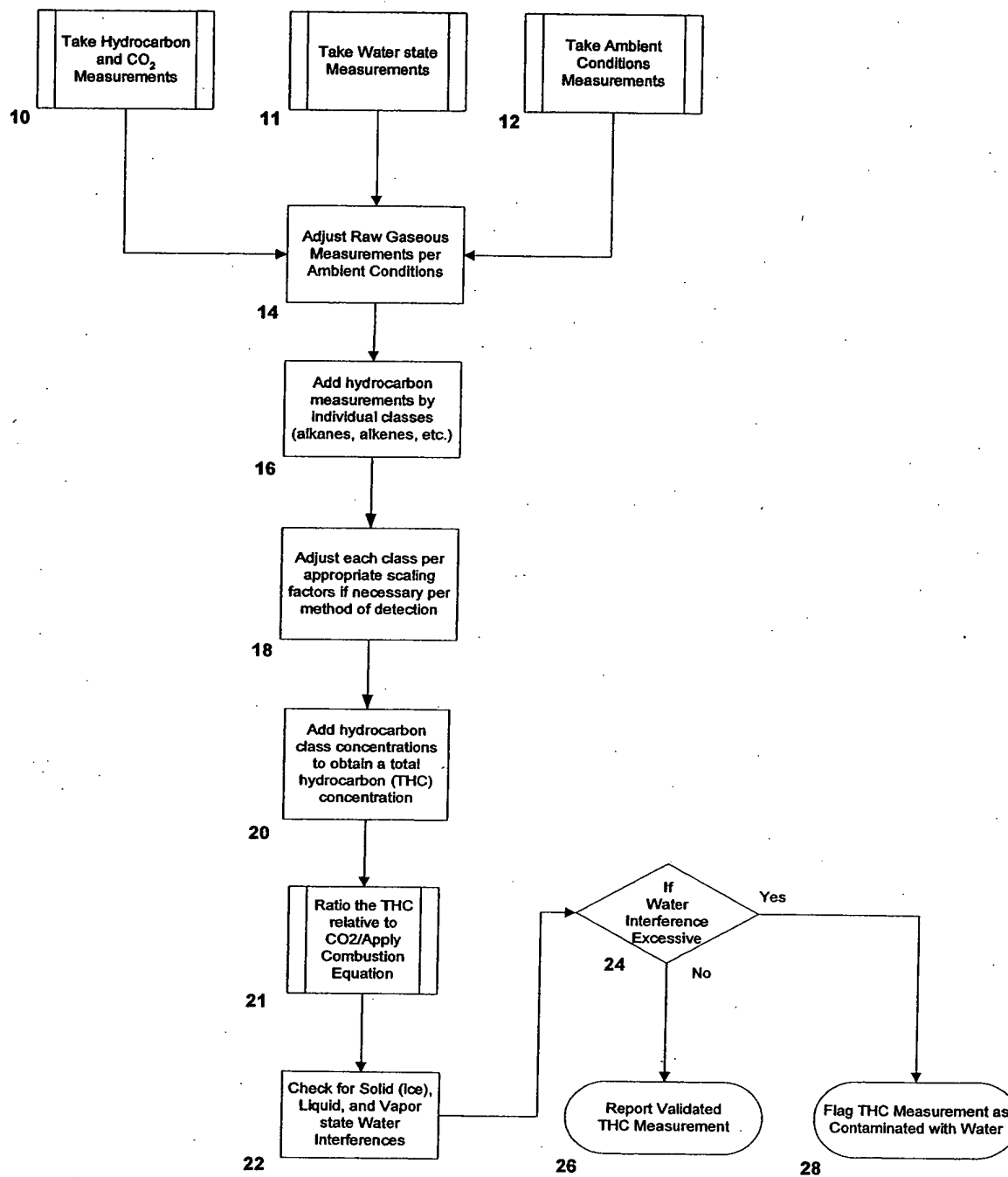


Fig. 1

The diagram illustrates a system architecture with a central horizontal bus labeled 94. Components are connected to this bus as follows:

- Top Row (Left to Right):**
 - Detection Unit (90):** Connected to bus 94 via a downward arrow.
 - Instruction Memory (96):** Connected to bus 94 via a downward arrow.
 - Permanent Data Storage Memory (106):** Connected to bus 94 via a downward arrow.
 - Additional Memory (108):** Connected to bus 94 via a downward arrow.
 - Display (110):** Connected to bus 94 via a downward arrow.
 - Transmitter (112):** Connected to bus 94 via a downward arrow.
- Bottom Row (Left to Right):**
 - Input (93):** Connected to bus 94 via an upward arrow.
 - Processor (92):** Connected to bus 94 via an upward arrow.
 - Receiver (95):** Connected to bus 94 via an upward arrow.
 - Ambient Conditions Input (114):** Connected to bus 94 via an upward arrow.
- Other Connections:**
 - A dashed line labeled 100 connects the **Input (93)** block to the **Remote Detection Unit (91)**.
 - Three unlabeled lines, labeled 101, 102, and 103, connect the **Remote Detection Unit (91)** to the bus 94.

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